



TFT LCD Tentative Specification

MODEL NO.: V546H1 - LE2

Customer: _____

Approved by: _____

Note:

Approved By	TVHD	
	LY Chen	

Reviewed By	QA Dept.	Product Development Div.
	Hsin-nan Chen	WT Lin

Prepared By	LCD TV Marketing and Product Management Div.	
	CY Chang	Lily Yang



CONTENTS -

REVISION HISTORY	3
1. GENERAL DESCRIPTION	4
1.1 OVERVIEW	4
1.2 FEATURES	4
1.3 APPLICATION	4
1.4 GENERAL SPECIFICATIONS	4
1.5 MECHANICAL SPECIFICATIONS	4
2. ABSOLUTE MAXIMUM RATINGS	5
2.1 ABSOLUTE RATINGS OF ENVIRONMENT	5
2.2 ELECTRICAL ABSOLUTE RATINGS	6
3. ELECTRICAL CHARACTERISTICS	7
3.1 TFT LCD MODULE (Ta = 25 ± 2 °C)	7
3.2 BACKLIGHT CONVERTER UNIT	9
4. BLOCK DIAGRAM OF INTERFACE	11
4.1 TFT LCD MODULE	11
5 .INPUT TERMINAL PIN ASSIGNMENT	12
5.1 TFT LCD Module	12
5.2 CONVERTER UNIT	15
5.3 BLOCK DIAGRAM OF INTERFACE	16
5.4 LVDS INTERFACE	18
5.5 COLOR DATA INPUT ASSIGNMENT	19
6. INTERFACE TIMING	20
6.1 INPUT SIGNAL TIMING SPECIFICATIONS	20
6.2 POWER ON/OFF SEQUENCE	21
7. OPTICAL CHARACTERISTICS	22
7.1 TEST CONDITIONS	22
7.2 OPTICAL SPECIFICATIONS	22
8. DEFINITION OF LABELS	26
8.1 CMO MODULE LABEL	26
9. PACKING	27
9.1 PACKING SPECIFICATIONS	27
9.2 PACKING METHOD	27
10. PRECAUTIONS	29
10.1 ASSEMBLY AND HANDLING PRECAUTIONS	29
10.2 SAFETY PRECAUTIONS	29
10.3 SAFETY STANDARDS	29
11. MECHANICAL CHARACTERISTIC	30

**CHI MEI**
OPTOELECTRONICS CORP.

Issued Date: June 25, 2009

Model No.: V546H1-LE2

Tentative**REVISION HISTORY**

Version	Date	Page (New)	Section	Description

1. GENERAL DESCRIPTION

1.1 OVERVIEW

V546H1-LE2 is a 54.6" TFT Liquid Crystal Display module with LED Backlight unit and 4ch-LVDS interface.

This module supports 1920 x 1080 HDTV format and can display true 1.073G colors (8bit+FRC/color). The Converter module for backlight is built-in.

1.2 FEATURES

- High brightness (450nits)
- High contrast ratio (4000:1)
- Fast response time (Gray to Gray typical 4.5ms)
- High color saturation (72% NTSC)
- Full HDTV (1920 x 1080 pixels) resolution, true HDTV format
- DE (Data Enable) only mode
- LVDS (Low Voltage Differential Signaling) interface
- Optimized response time for 100/120 Hz frame rate
- Ultra wide viewing angle: Super MVA technology

1.3 APPLICATION

- Standard Living Room TVs.
- Public Display Application.
- Home Theater Application.
- MFM Application.

1.4 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Active Area	1209.6(H) x 680.4(V) (54.6" diagonal)	mm	(1)
Bezel Opening Area	1217.6 (H) x 688.4 (V)	mm	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1920x R.G.B. x 1080	pixel	-
Pixel Pitch(Sub Pixel)	0.21(H) x 0.63(V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	1.073G	color	-
Display Operation Mode	Transmissive mode / Normally black	-	-
Surface Treatment	Anti-Glare coating (11% Low Haze) Hardness (3H)	-	(2)

Note (1) Please refer to the attached drawings in chapter 9 for more information about the front and back outlines.

Note (2) The spec of the surface treatment is temporarily for this phase. CMO reserves the rights to change this feature.

1.5 MECHANICAL SPECIFICATIONS

Item	Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	1266.1	1267.6	1269.1	mm (1), (2)
	Vertical (V)	737.2	738.4	739.6	
	Depth (D)	38.5	40	41.5	
Weight	-	21500	-	g	-

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

Note (2) Module Depth does not include connectors.

2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T _{ST}	-20	+60	°C	(1)
Operating Ambient Temperature	T _{OP}	0	50	°C	(1), (2)
Shock (Non-Operating)	S _{NOP}	-	30	G	(3), (5)
			30		
Vibration (Non-Operating)	V _{NOP}	-	1.0	G	(4), (5)

Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. ($T_a \leq 40$ °C).

(b) Wet-bulb temperature should be 39 °C Max. ($T_a > 40$ °C).

(c) No condensation.

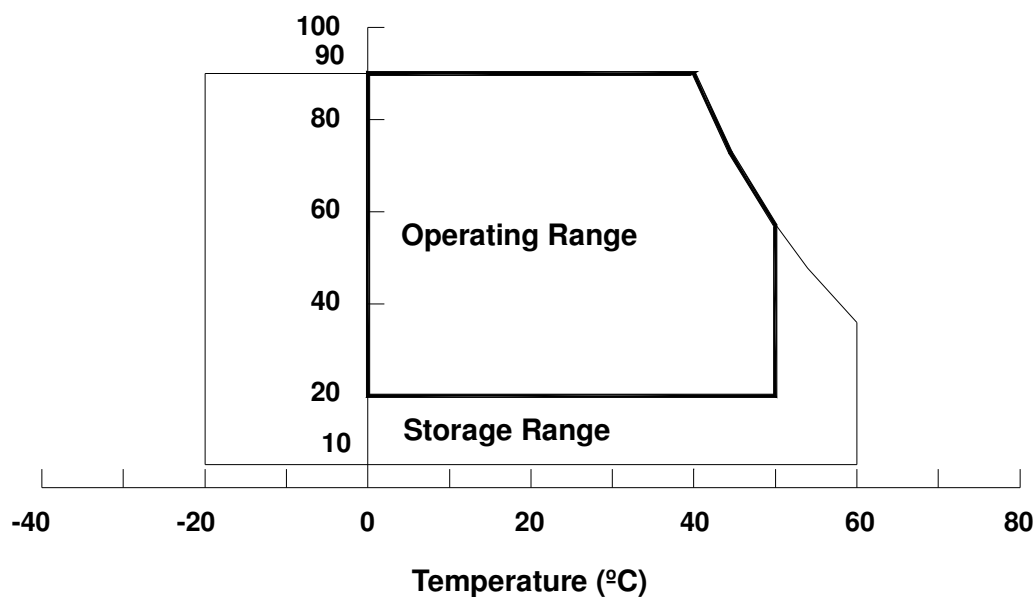
Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65 °C with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 65 °C. The range of operating temperature may degrade in case of improper thermal management in final product design.

Note (3) 11 ms, half sine wave, 1 time for $\pm X$, $\pm Y$, $\pm Z$.

Note (4) 10 ~ 200 Hz, 10 min, 1 time each X, Y, Z.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

Relative Humidity (%RH)



2.2 ELECTRICAL ABSOLUTE RATINGS

2.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	V_{CC}	-0.3	13.5	V	(1)
Logic Input Voltage	V_{IN}	-0.3	3.6	V	

2.2.2 BACKLIGHT UNIT

Item	Symbol	Test Condition	Min.	Type	Max.	Unit	Note
Light Bar Voltage	V_W	$T_a = 25\text{ }^{\circ}\text{C}$	-	-	60	V_{RMS}	
Converter Input Voltage	V_{BL}	-	0	-	30	V	
Control Signal Level	-	-	-0.3	-	7	V	

Note(1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

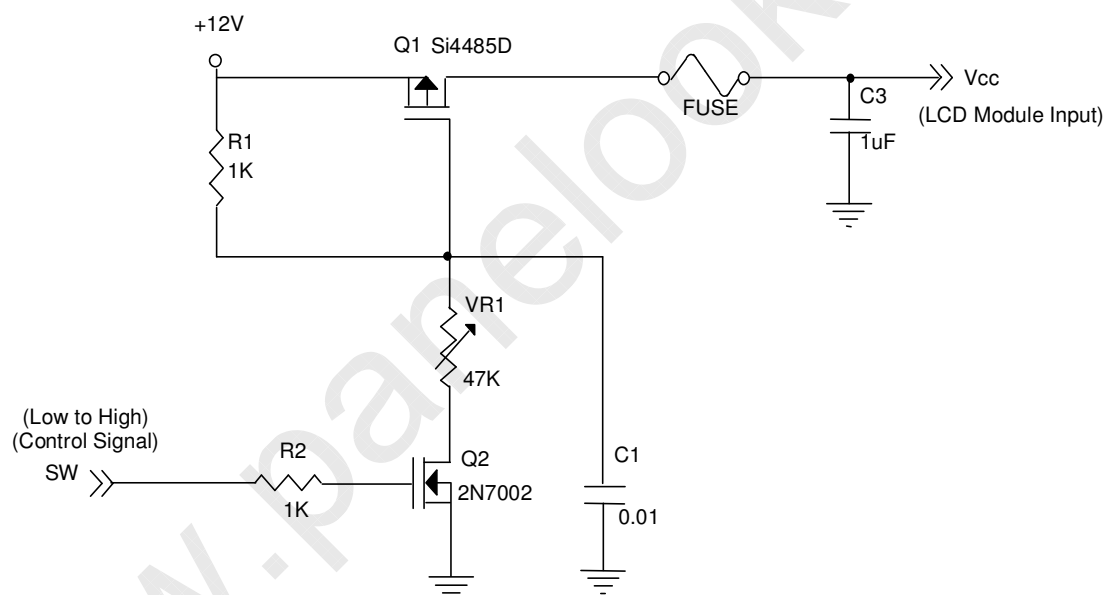
3. ELECTRICAL CHARACTERISTICS

3.1 TFT LCD MODULE ($T_a = 25 \pm 2^\circ\text{C}$)

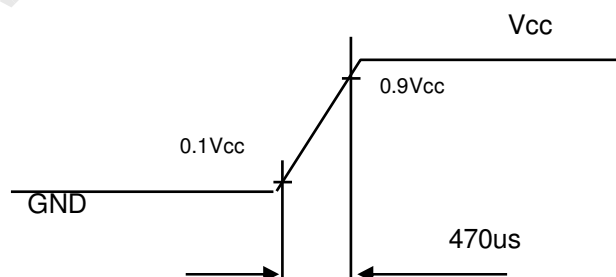
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V_{CC}	10.8	12.0	13.2	V	(1)
Power Supply Ripple Voltage		V_{RP}	-	-	350	mV	
Rush Current		I_{RUSH}	-	TBD	TBD	A	(2)
Power Supply Current	White	-	-	TBD	TBD	A	(3)
	Black	-	-	TBD	TBD	A	
	Horizontal one line stripe	-	-	TBD	TBD	A	
LVDS Interface	Common Input Voltage	V_{LVC}	1.125	1.25	1.375	V	
	Terminating Resistor	R_T	-	100	-	ohm	
CMOS interface	Input High Threshold Voltage	V_{IH}	2.7	-	3.3	V	
	Input Low Threshold Voltage	V_{IL}	0	-	0.7	V	

Note (1) The module should be always operated within the above ranges.

Note (2) Measurement condition:



Vcc rising time is 470us



Note (3) The specified power supply current is under the conditions at $V_{CC} = 12\text{V}$, $T_a = 25 \pm 2^\circ\text{C}$, $f_v = 120\text{ Hz}$, whereas a power dissipation check pattern below is displayed.



CHI MEI
OPTOELECTRONICS CORP.

Issued Date: June 25, 2009

Model No.: V546H1-LE2

Tentative

a. White Pattern



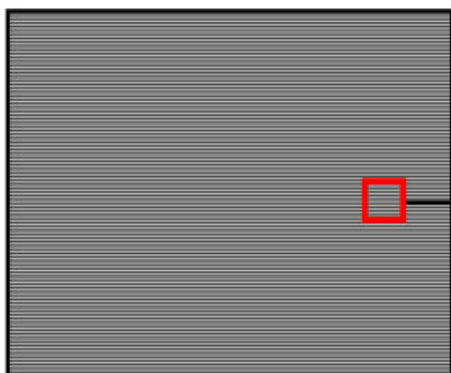
Active Area

b. Black Pattern



Active Area

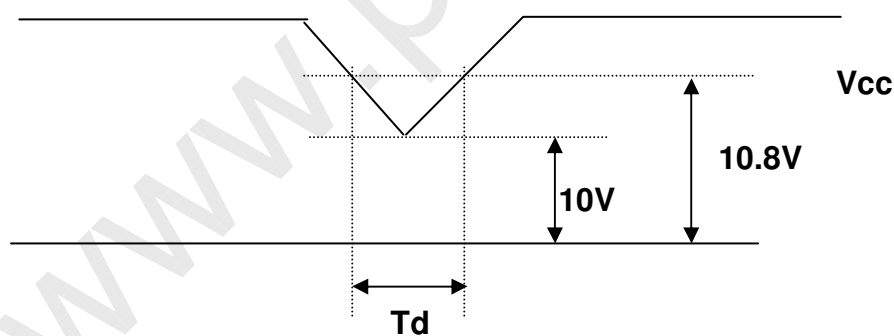
c. Horizontal one line stripe



Active Area



3.1.2 Vcc Power Dip Condition:



Dip condition: $10V \leq V_{cc} \leq 10.8V$, $T_d \leq 20ms$

3.2 BACKLIGHT CONVERTER UNIT

3.2.1 LED LIGHT BAR CHARACTERISTICS (Ta = 25 ± 2 °C)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Light Bar Voltage	V _W	-	-	30.6	V _{RMS}	I _L = 50mA
Forward Voltage	V _f	3.0	3.2	3.4	V _{RMS}	I _L = 50mA
LED Current	I _L	TBD	50	TBD	mA _{RMS}	

3.2.2 CONVERTER CHARACTERISTICS (Ta = 25 ± 2 °C)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Power Consumption	P _{BL}	-	212	TBD	W	
Inverter Input Voltage	V _{BL}	22.8	24	25.2	V _{DC}	
Inverter Input Current	I _{BL}	-	8.8	-	A	I _L = 50mA, Duty = 100%
Oscillating Frequency	F _W	120	150	180	kHz	
Dimming Frequency	F _B	150	160	170	Hz	User Dimming
Minimum Duty Ratio	D _{MIN}	-	5	-	%	

3.2.3 CONVERTER INTERFACE CHARACTERISTICS

Parameter		Symbol	Test Condition	Value			Unit	Note
				Min.	Typ.	Max.		
On/Off Control Voltage	ON	VBLON	—	2.0	—	5.0	V	
	OFF		—	0	—	0.8	V	
Internal PWM Control Voltage	MAX	VIPWM	—	3.15	—	3.45	V	maximum duty ratio
	MIN		—	—	0	—	V	minimum duty ratio
External PWM Control Voltage	HI	VEPWM	—	2.0	—	5.0	V	Duty on
	LO		—	0	—	0.8	V	Duty off
Status Signal	HI	Status	—	3.0	3.3	3.6	V	Normal
	LO		—	0	—	0.8	V	Abnormal
VBL Rising Time		Tr1	—	30	—	—	ms	10%-90%V _{BL}
VBL Falling Time		Tf1	—	30	—	—	ms	
Control Signal Rising Time		Tr	—	—	—	100	ms	
Control Signal Falling Time		Tf	—	—	—	100	ms	
PWM Signal Rising Time		TPWMR	—	—	—	50	us	
PWM Signal Falling Time		TPWMF	—	—	—	50	us	
Input Impedance		Rin	—	1	—	—	MΩ	

PWM Delay Time	TPWM	—	100	—	—	ms	
BLON Delay Time	T _{on}	—	300	—	—	ms	
	T _{on1}	—	300	—	—	ms	
BLON Off Time	Toff	—	300	—	—	ms	

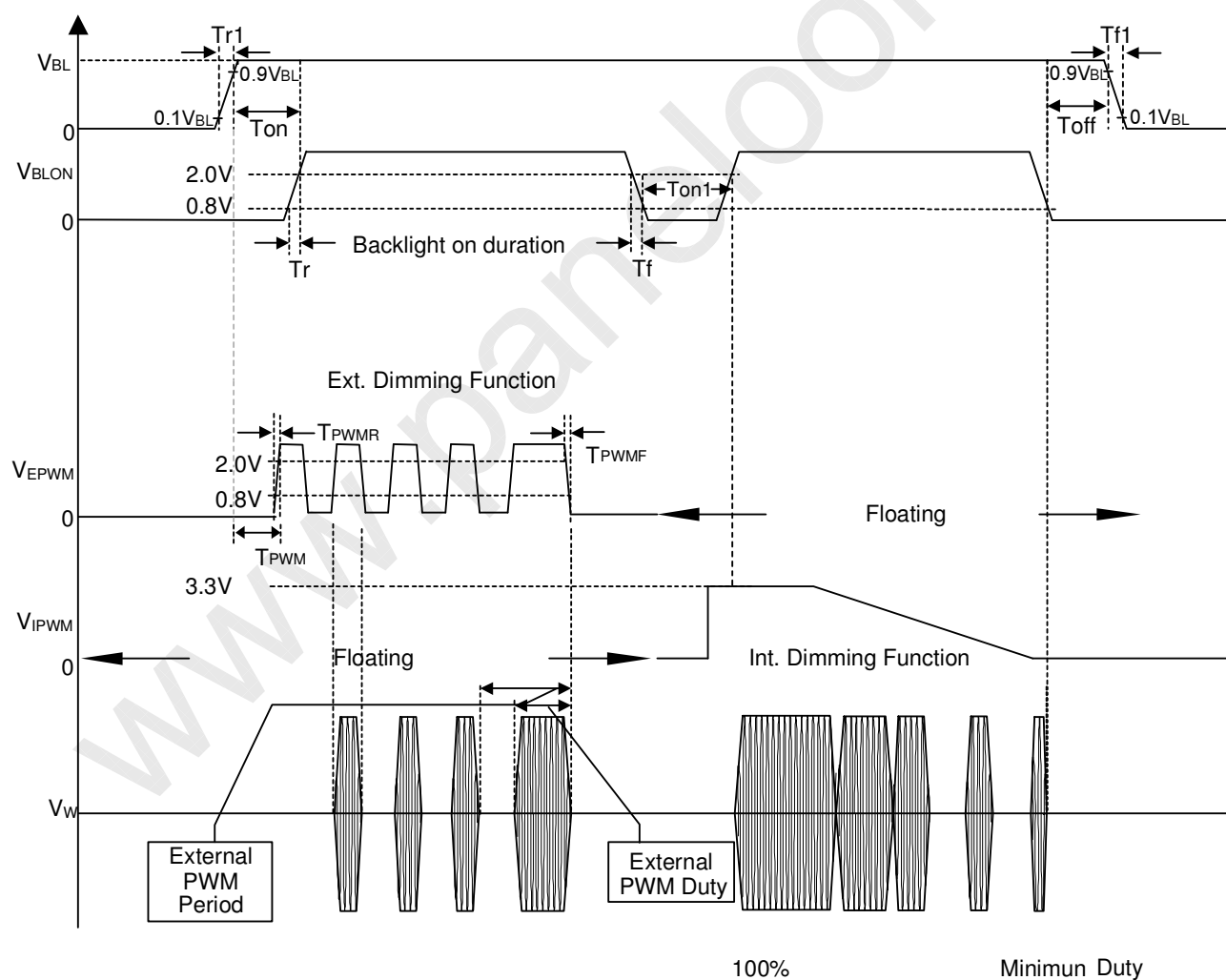
Note (1) The Dimming signal should be valid before backlight turns on by BLON signal. It is inhibited to change the internal/external PWM signal during backlight turn on period.

Note (2) The power sequence and control signal timing are shown in the following figure. For a certain reason, the converter has a possibility to be damaged with wrong power sequence and control signal timing.

Note (3) While system is turned ON or OFF, the power sequences must follow as below descriptions:

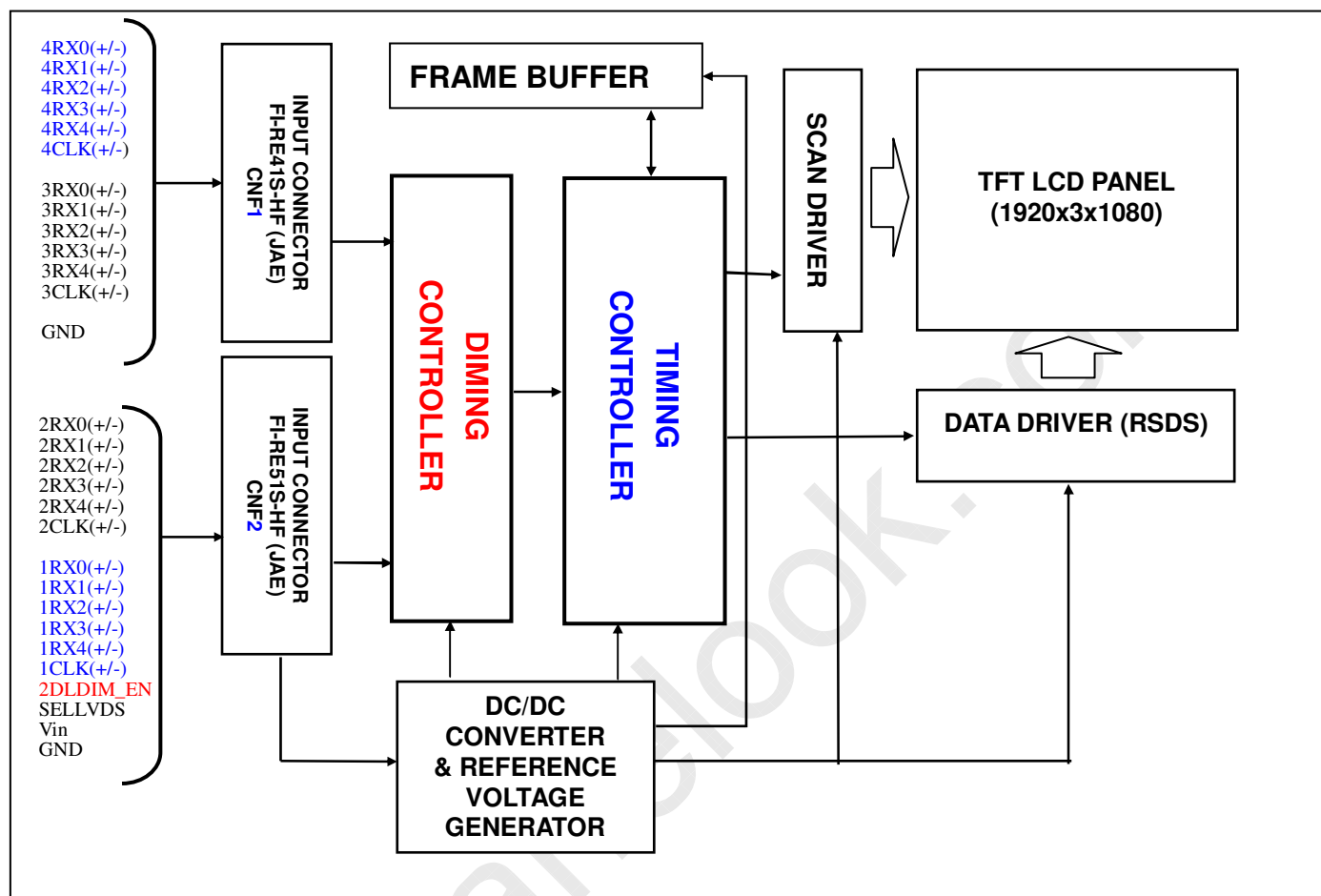
Turn ON sequence: VBL → PWM signal → BLON

Turn OFF sequence: BLOFF → PWM signal → VBL



4. BLOCK DIAGRAM OF INTERFACE

4.1 TFT LCD MODULE



5 .INPUT TERMINAL PIN ASSIGNMENT

5.1 TFT LCD Module

CNF1 Connector Pin Assignment (FI-RE41S-HF (JAE) or equivalent)

Pin	Name	Description	Note
1	GND	Ground	
2	N.C.	No Connection	(1)
3	N.C.	No Connection	
4	N.C.	No Connection	
5	N.C.	No Connection	
6	N.C.	No Connection	
7	N.C.	No Connection	
8	N.C.	No Connection	
9	GND	Ground	
10	CH3_0N	Third Pixel Negative LVDS differential data input. Channel 0	(4)
11	CH3_0P	Third Pixel Positive LVDS differential data input. Channel 0	
12	CH3_1N	Third Pixel Negative LVDS differential data input. Channel 1	
13	CH3_1P	Third Pixel Positive LVDS differential data input. Channel 1	
14	CH3_2N	Third Pixel Negative LVDS differential data input. Channel 2	
15	CH3_2P	Third Pixel Positive LVDS differential data input. Channel 2	
16	GND	Ground	
17	CH3_CLKN	Third Pixel Negative LVDS differential clock input.	
18	CH3_CLKP	Third Pixel Positive LVDS differential clock input.	
19	GND	Ground	
20	CH3_3N	Third Pixel Negative LVDS differential data input. Channel 3	(4)
21	CH3_3P	Third Pixel Positive LVDS differential data input. Channel 3	
22	CH3_4N	Third Pixel Negative LVDS differential data input. Channel 4	
23	CH3_4P	Third Pixel Positive LVDS differential data input. Channel 4	
24	N.C.	No Connection	(1)
25	N.C.	No Connection	
26	CH4_0N	Fourth Pixel Negative LVDS differential data input. Channel 0	(4)
27	CH4_0P	Fourth Pixel Positive LVDS differential data input. Channel 0	
28	CH4_1N	Fourth Pixel Negative LVDS differential data input. Channel 1	
29	CH4_1P	Fourth Pixel Positive LVDS differential data input. Channel 1	
30	CH4_2N	Fourth Pixel Negative LVDS differential data input. Channel 2	
31	CH4_2P	Fourth Pixel Positive LVDS differential data input. Channel 2	
32	GND	Ground	
33	CH4_CLKN	Fourth Pixel Negative LVDS differential clock input.	
34	CH4_CLKP	Fourth Pixel Positive LVDS differential clock input.	
35	GND	Ground	
36	CH4_3N	Fourth Pixel Negative LVDS differential data input. Channel 3	(4)
37	CH4_3P	Fourth Pixel Positive LVDS differential data input. Channel 3	
38	CH4_4N	Fourth Pixel Negative LVDS differential data input. Channel 4	
39	CH4_4P	Fourth Pixel Positive LVDS differential data input. Channel 4	
40	N.C.	No Connection	(1)
41	N.C.	No Connection	

CNF2 Connector Pin Assignment (FI-RE51S-HF (JAE) or equivalent)

Pin	Name	Description	Note
1	N.C.	No Connection	(1)
2	N.C.	No Connection	
3	N.C.	No Connection	
4	N.C.	No Connection	
5	ODSEL	Overdrive Lookup Table Selection	(3)
6	N.C.	No Connection	(1)
7	SELLVDS	LVDS Data Format Selection	(2)
8	2DLDIM_EN	2D Local dimming ON/OFF	(3)
9	N.C.	No Connection	(1)
10	N.C.	No Connection	
11	GND	Ground	
12	CH1_0N	First Pixel Negative LVDS differential data input. Channel 0	(4)
13	CH1_0P	First Pixel Positive LVDS differential data input. Channel 0	
14	CH1_1N	First Pixel Negative LVDS differential data input. Channel 1	
15	CH1_1P	First Pixel Positive LVDS differential data input. Channel 1	
16	CH1_2N	First Pixel Negative LVDS differential data input. Channel 2	(4)
17	CH1_2P	First Pixel Positive LVDS differential data input. Channel 2	
18	GND	Ground	
19	CH1_CLKN	First Pixel Negative LVDS differential clock input.	
20	CH1_CLKP	First Pixel Positive LVDS differential clock input.	
21	GND	Ground	
22	CH1_3N	First Pixel Negative LVDS differential data input. Channel 3	(4)
23	CH1_3P	First Pixel Positive LVDS differential data input. Channel 3	
24	CH1_4N	First Pixel Negative LVDS differential data input. Channel 4	
25	CH1_4P	First Pixel Positive LVDS differential data input. Channel 4	
26	N.C.	No Connection	(1)
27	N.C.	No Connection	
28	CH2_0N	Second Pixel Negative LVDS differential data input. Channel 0	(4)
29	CH2_0P	Second Pixel Positive LVDS differential data input. Channel 0	
30	CH2_1N	Second Pixel Negative LVDS differential data input. Channel 1	
31	CH2_1P	Second Pixel Positive LVDS differential data input. Channel 1	
32	CH2_2N	Second Pixel Negative LVDS differential data input. Channel 2	(4)
33	CH2_2P	Second Pixel Positive LVDS differential data input. Channel 2	
34	GND	Ground	
35	CH2_CLKN	Second Pixel Negative LVDS differential clock input.	
36	CH2_CLKP	Second Pixel Positive LVDS differential clock input.	
37	GND	Ground	
38	CH2_3N	Second Pixel Negative LVDS differential data input. Channel 3	(4)
39	CH2_3P	Second Pixel Positive LVDS differential data input. Channel 3	
40	CH2_4N	Second Pixel Negative LVDS differential data input. Channel 4	
41	CH2_4P	Second Pixel Positive LVDS differential data input. Channel 4	
42	N.C.	No Connection	(1)
43	N.C.	No Connection	
44	GND	Ground	


CHI MEI
 OPTOELECTRONICS CORP.

Issued Date: June 25, 2009

Model No.: V546H1-LE2

Tentative

45	GND	Ground	
46	GND	Ground	
47	N.C.	No Connection	(1)
48	Vin	Power input (+12V)	
49	Vin	Power input (+12V)	
50	Vin	Power input (+12V)	
51	Vin	Power input (+12V)	

Note (1) Please be reserved to open.

Note (2) Low or Open: VESA Format(default), connect to GND. High: JEIDA Format, connect to +3.3V.

Note (3) Local dimming function selection

2DLDIM_EN	Backlight Status
L (GND or Open)	Full on
H (+3.3V)	2D Dimming

Note (4) LVDS 4-Port Data Mapping

Port	CH of LVDS	Data Stream
1st Port	First pixel	1, 5, 9,, 1913, 1917
2nd Port	Second pixel	2, 6, 10,, 1914, 1918
3rd Port	Third pixel	3, 7, 11,, 1915, 1919
4th Port	Fourth pixel	4, 8, 12,, 1916, 1920

Note (5) Low : function disable (default), High : Dynamic Contrast Ratio function enable

5.2 CONVERTER UNIT

CN1(Header): CI0114M1HR0-LF (CviLux) at Master Board

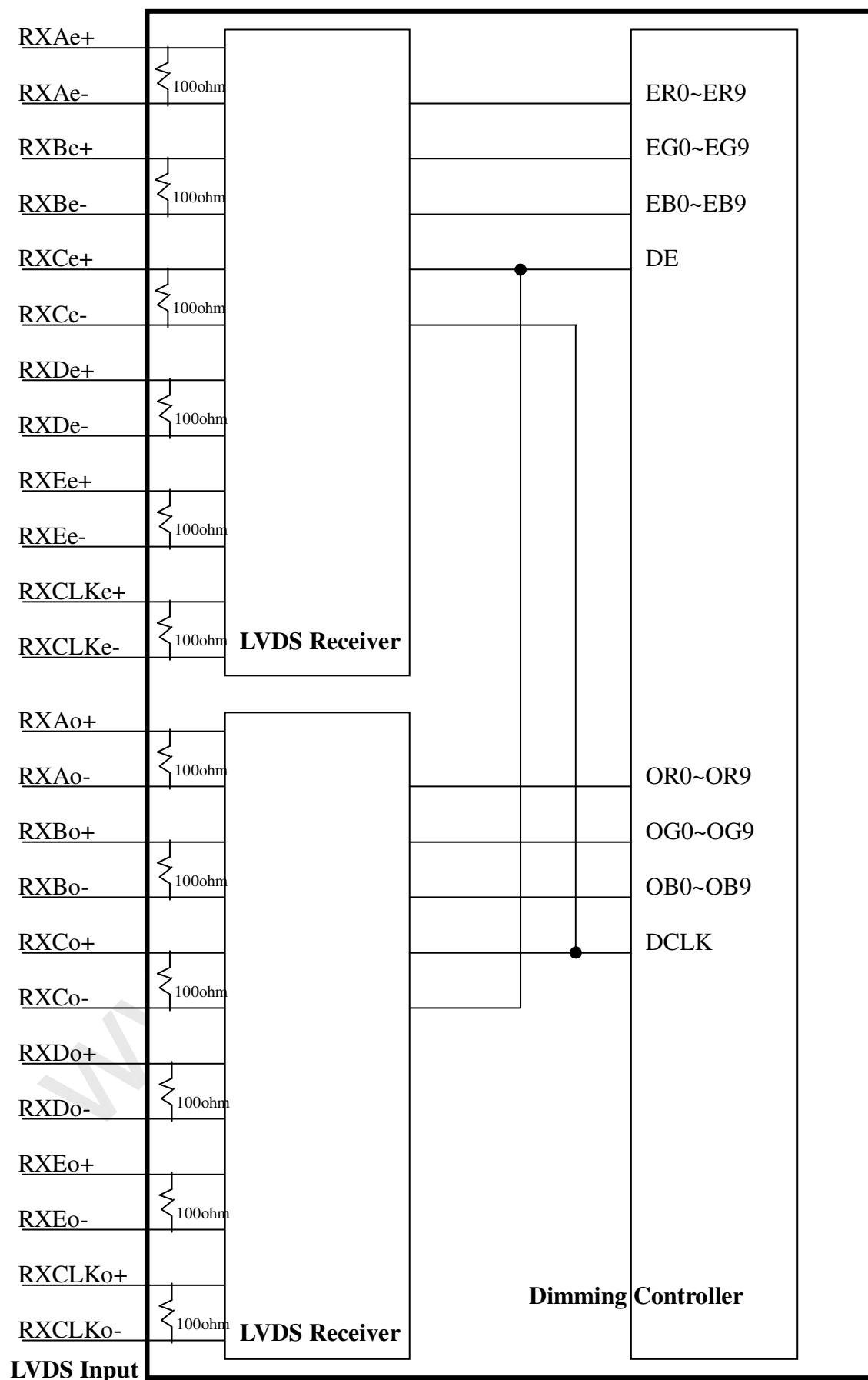
Pin №	Symbol	Feature
1	VBL	+24V
2		
3		
4		
5		
6	GND	GND
7		
8		
9		
10		
11	Status	Normal (3.3V) Abnormal (0V)
12	E_PWM	External PWM Control
13	I_PWM	Internal PWM Control
14	BLON	BL ON/OFF

CN2: CI0112M1HR0-LF (CviLux) at Slave Board

Pin №	Symbol	Feature
1	VBL	+24V
2		
3		
4		
5		
6	GND	GND
7		
8		
9		
10		
11	NC	NC
12	NC	NC

Signal of Video Processor to Converter's Connector

5.3 BLOCK DIAGRAM OF INTERFACE





CHI MEI
OPTOELECTRONICS CORP.

Issued Date: June 25, 2009

Model No.: V546H1-LE2

Tentative

ER0~ER9 : Even pixel R data

EG0~EG9 : Even pixel G data

EB0~EB9 : Even pixel B data

OR0~OR9 : Odd pixel R data

OG0~OG9 : Odd pixel G data

OB0~OB9 : Odd pixel B data

DE : Data enable signal

DCLK : Data clock signal

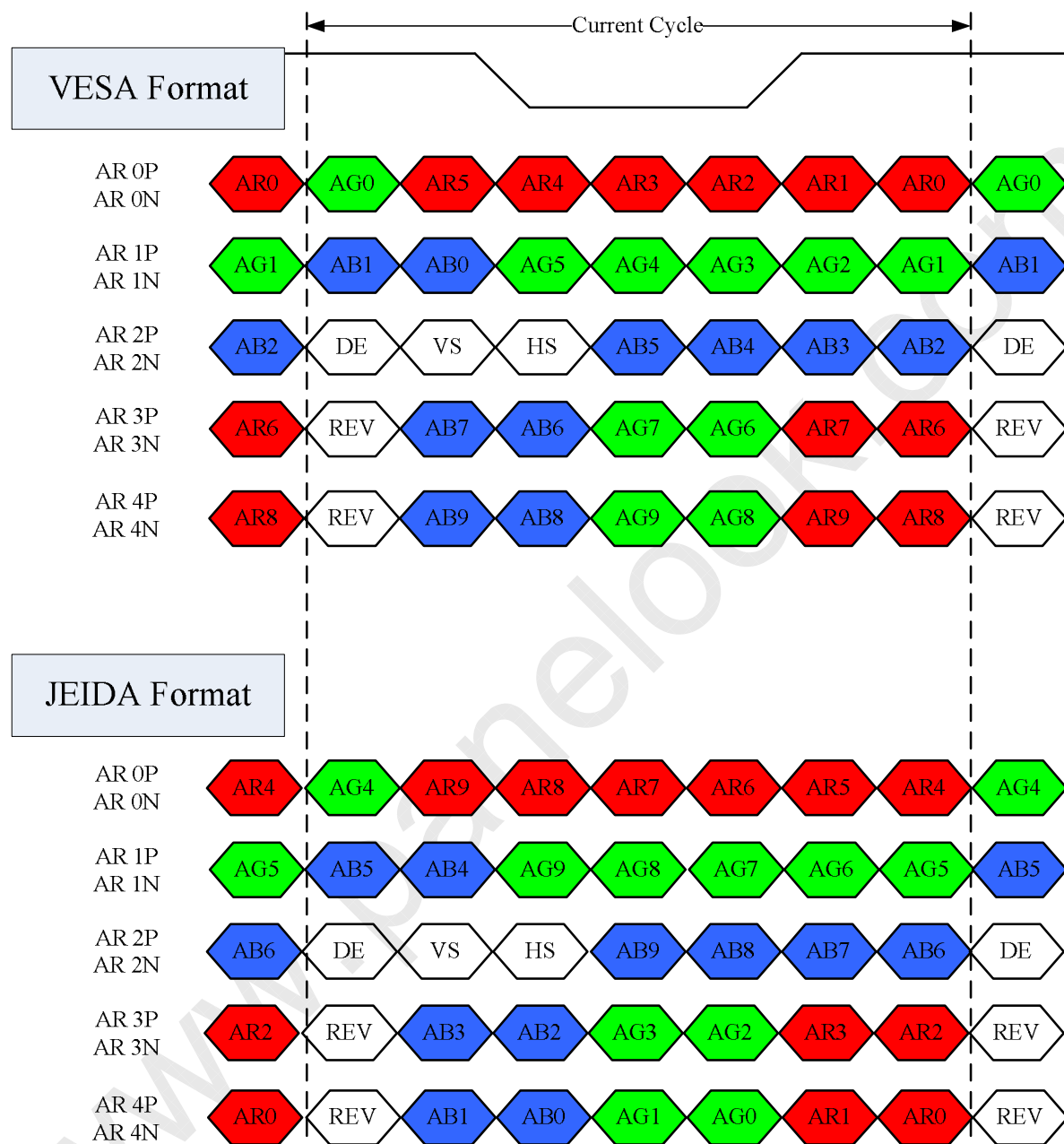
Note (1) The system must have the transmitter to drive the module.

Note (2) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line when it is used differentially.

5.4 LVDS INTERFACE

VESA Format : SELLVDS = L or Open

JEIDA Format : SELLVDS = H



AR0~AR9: First Pixel R Data (9; MSB, 0; LSB)

AG0~AG9: First Pixel G Data (9; MSB, 0; LSB)

AB0~AB9: First Pixel B Data (9; MSB, 0; LSB)

DE : Data enable signal

DCLK : Data clock signal

RSVD : Reserved


CHI MEI
OPTOELECTRONICS CORP.

Issued Date: June 25, 2009

Model No.: V546H1-LE2

Tentative

5.5 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 10-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																												
		Red										Green										Blue								
R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (2)	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red (1021)	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1022)	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green (1021)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0
	Green (1022)	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
	Green (1023)	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue (1021)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1
	Blue (1022)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0
	Blue (1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

6. INTERFACE TIMING

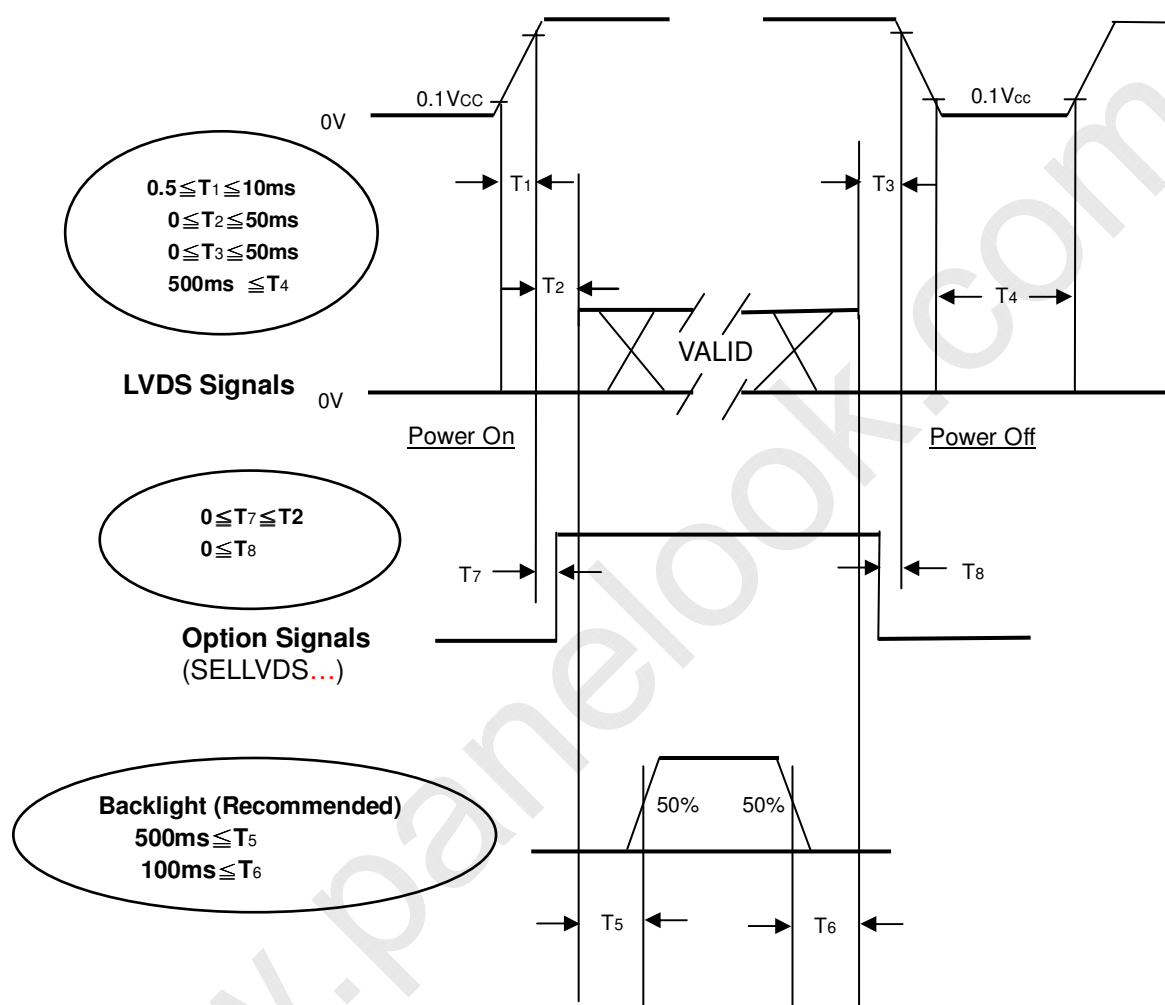
6.1 INPUT SIGNAL TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	1/Tc	60	74.25	78	MHz	-
	Input cycle to cycle jitter	Trcl	-	-	200	ps	-
LVDS Receiver Data	Setup Time	Tlvsu	600	-	-	ps	-
	Hold Time	Tlvhd	600	-	-	ps	-
Vertical Active Display Term	Frame Rate	Fr		120 100		Hz	-
	Total	Tv	1115	1125	1135	Th	Tv=Tvd+Tvb
	Display	Tvd	1080	1080	1080	Th	-
	Blank	Tvb	35	45	55	Th	-
Horizontal Active Display Term	Total	Th	525	550	575	Tc	Th=Thd+Thb
	Display	Thd	480	480	480	Tc	4ch-LVDS interface
	Blank	Thb	45	70	95	Tc	-

6.2 POWER ON/OFF SEQUENCE

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should follow the diagram below.



Power ON/OFF Sequence

Note:

- (1) The supply voltage of the external system for the module input should follow the definition of V_{CC}.
- (2) Apply the lamp voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.
- (3) In case of V_{CC} is in off level, please keep the level of input signals on the low or high impedance.
- (4) T₄ should be measured after the module has been fully discharged between power off and on period.
- (5) Interface signal shall not be kept at high impedance when the power is on.

7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V _{CC}	12V	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
LED Current	I _L	50.0±	mA

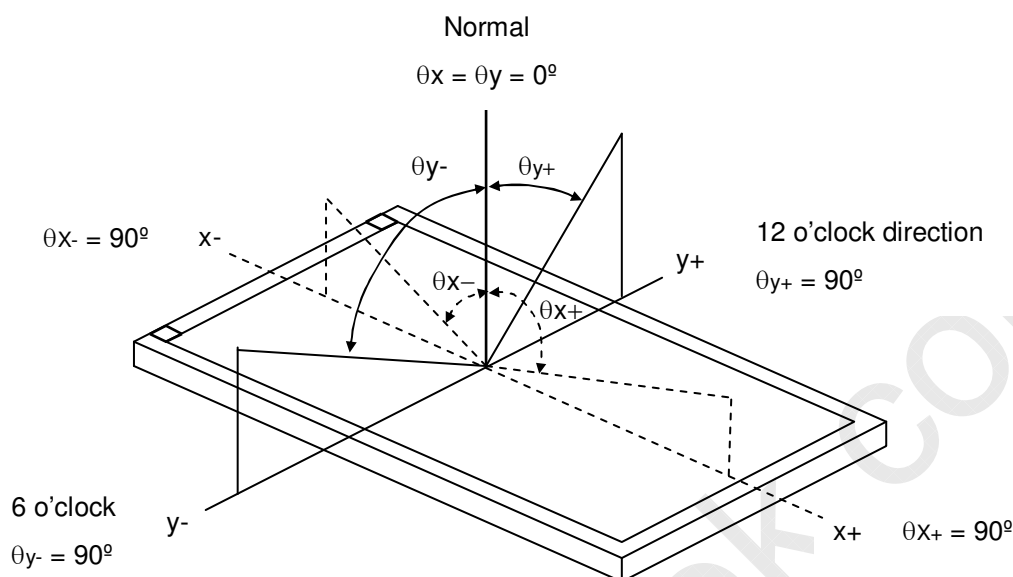
7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in Note (6).

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	$\theta_x=0^\circ, \theta_Y=0^\circ$ Viewing angle at normal direction	3000	4000	-	-	Note (2)
Response Time		Gray to gray		-	4.5	9	ms	Note (3)
Center Luminance of White		L _C		350	450	-	cd/m ²	Note (4)
White Variation		δW		-	-	1.3	-	Note (7)
Cross Talk		CT		-	-	4	%	Note (5)
Color Chromaticity	Red	R _x		Typ.- 0.03	0.634	Typ.+ 0.03	-	Note (6)
		R _y			0.331		-	
	Green	G _x			0.294		-	
		G _y			0.598		-	
	Blue	B _x			0.150		-	
		B _y	0.058		-			
	White	W _x	0.280		-			
		W _y	0.290		-			
	Color Gamut				76		80	
Viewing Angle	Horizontal	θ _{x+}	CR≥20	80	88	-	Deg.	Note (1)
		θ _{x-}		80	88	-		
	Vertical	θ _{y+}		80	88	-		
		θ _{y-}		80	88	-		

Note (1) Definition of Viewing Angle (θ_x, θ_y):

Viewing angles are measured by Eldim EZ-Contrast 160R



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

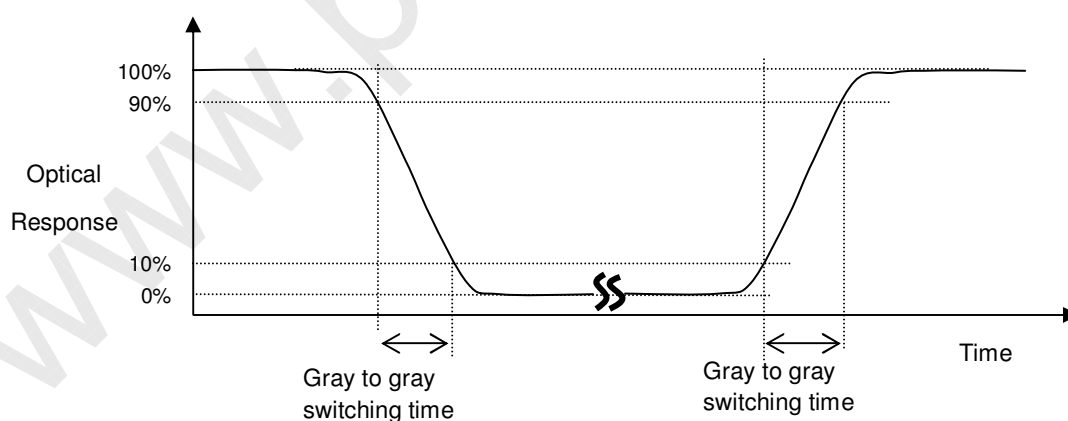
$$\text{Contrast Ratio (CR)} = L_{255} / L_0$$

L255: Luminance of gray level 255

L 0: Luminance of gray level 0

CR = CR (5), where CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (7)

Note (3) Definition of Gray to Gray Switching Time :



The driving signal means the signal of gray level 0, 63, 127, 191, and 255.

Gray to gray average time means the average switching time of gray level 0, 63, 127, 191, 255 to each other.

Note (4) Definition of Luminance of White (L_C):

Measure the luminance of gray level 255 at center point.

$L_C = L(5)$, where $L(x)$ is corresponding to the luminance of the point X at the figure in Note (7).

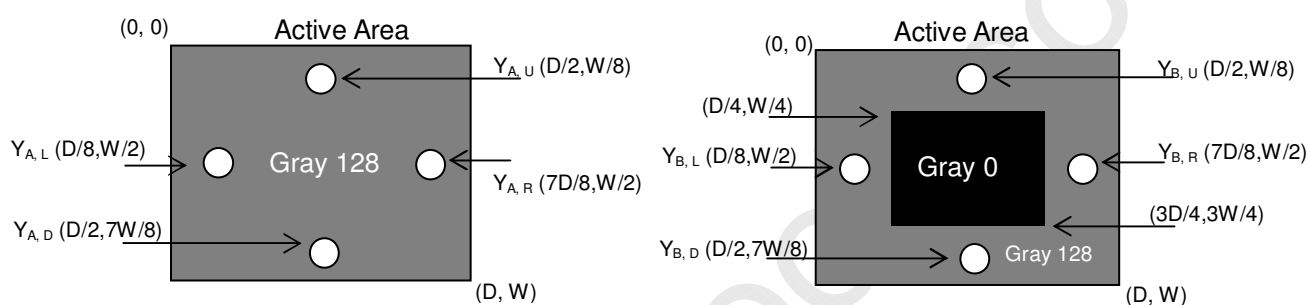
Note (5) Definition of Cross Talk (CT):

$$CT = |Y_B - Y_A| / Y_A \times 100 (\%)$$

Where:

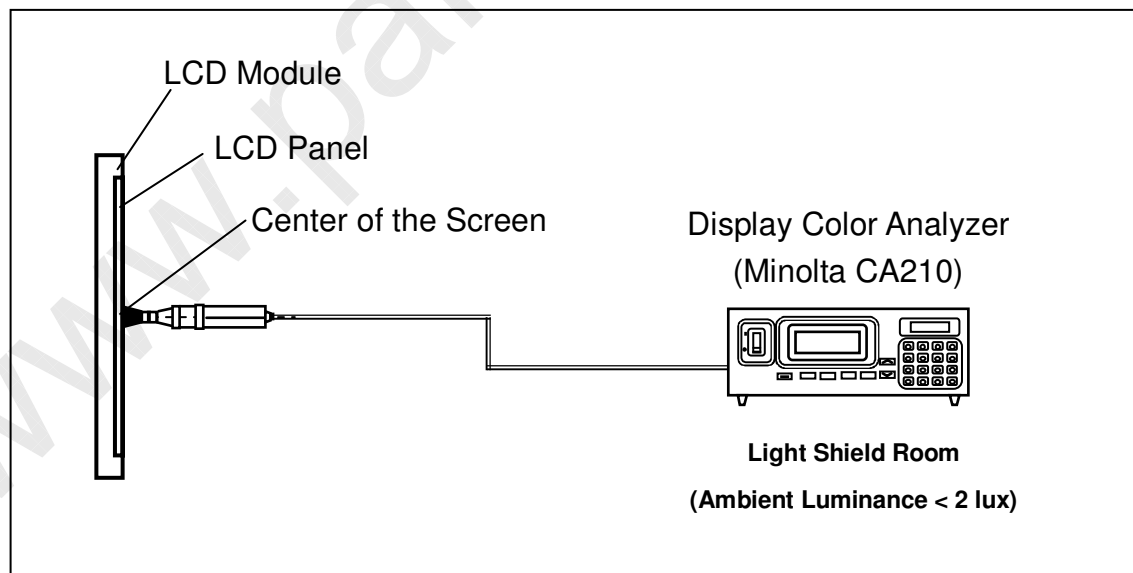
Y_A = Luminance of measured location without gray level 255 pattern (cd/m^2)

Y_B = Luminance of measured location with gray level 255 pattern (cd/m^2)



Note (6) Measurement Setup:

The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 1 hour in a windless room.



Note (7) Definition of White Variation (δW):

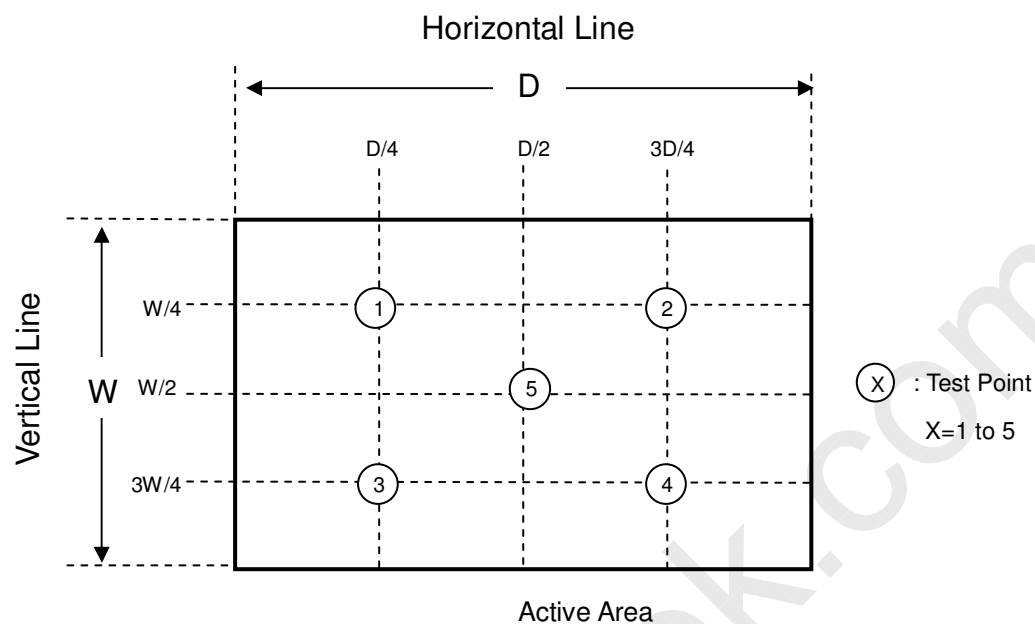
Measure the luminance of gray level 255 at 5 points

$$\delta W = \text{Maximum} [L(1), L(2), L(3), L(4), L(5)] / \text{Minimum} [L(1), L(2), L(3), L(4), L(5)]$$

**CHI MEI**
OPTOELECTRONICS CORP.

Issued Date: June 25, 2009

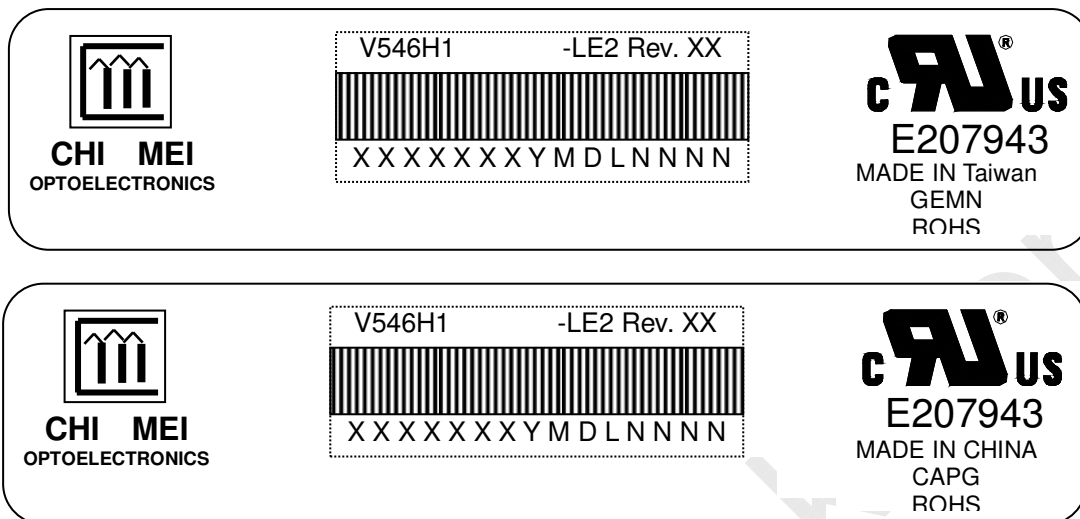
Model No.: V546H1-LE2

Tentative

8. DEFINITION OF LABELS

8.1 CMO MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



- (a) Model Name: V546H1-LE2
- (b) Revision: Rev. XX, for example: A0, A1... B1, B2... or C1, C2...etc.
- (c) CMO barcode definition:

Serial ID: XX-XX-X-XX-YMD-L-NNNN

Code	Meaning	Description
XX	CMO internal use	-
XX	Revision	Cover all the change
X-XX	CMO internal use	-
YMD	Year, month, day	Year: 2001=1, 2002=2, 2003=3, 2004=4... Month: Jan. ~ Dec.=1, 2, 3, ~, 9, A, B, C Day: 1 st to 31 st =1, 2, 3, ~, 9, A, B, C, ~, W, X, Y, exclude I, O, and U
L	Product line #	Line 1=1, Line 2=2, Line 3=3, ...
NNNN	Serial number	Manufacturing sequence of product

9. PACKING

9.1 PACKING SPECIFICATIONS

- (1) 2 LCD TV modules / 1 Box
- (2) Box dimensions: 1334(L) X 284 (W) X 856 (H)
- (3) Weight: approximately 46 Kg (2 modules per box)

9.2 PACKING METHOD

Figures 9-1 and 9-2 are the packing method

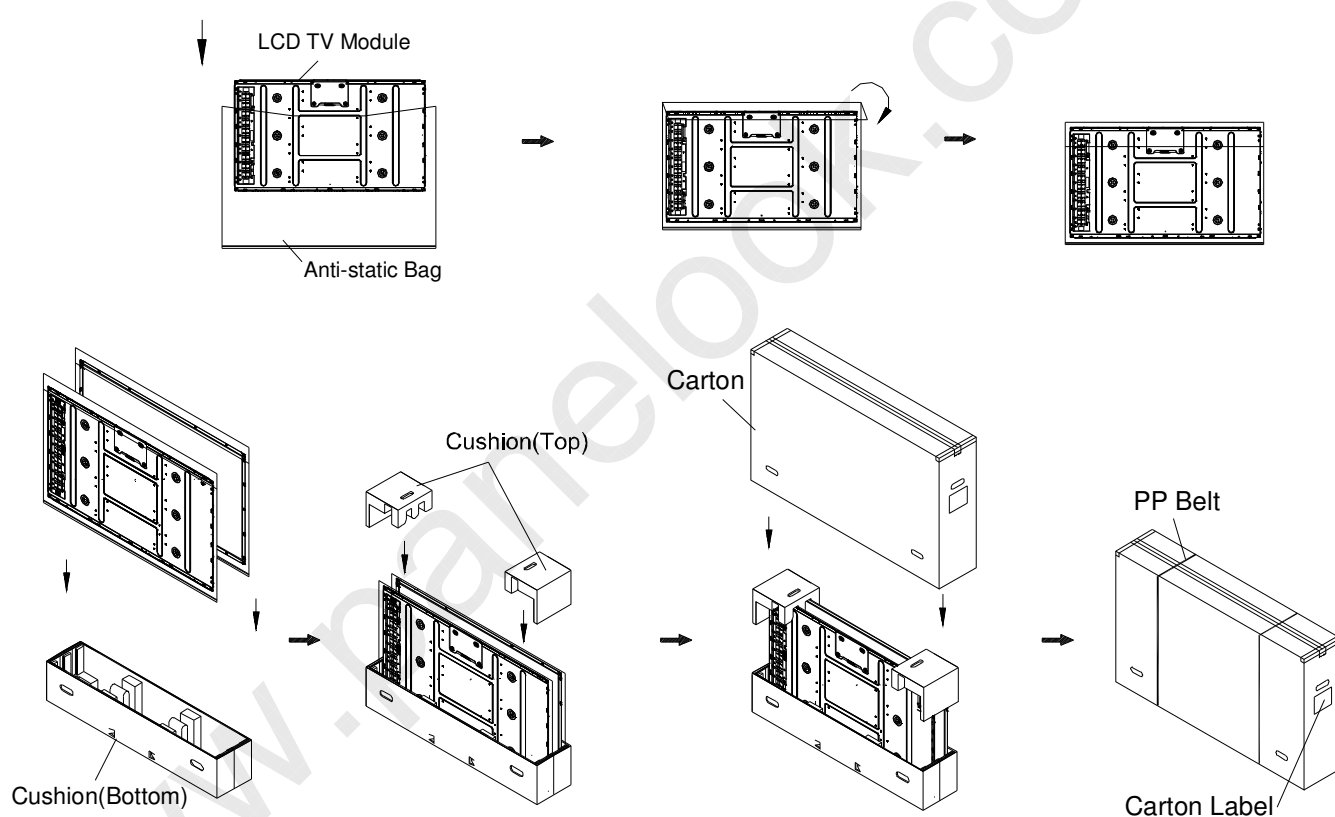
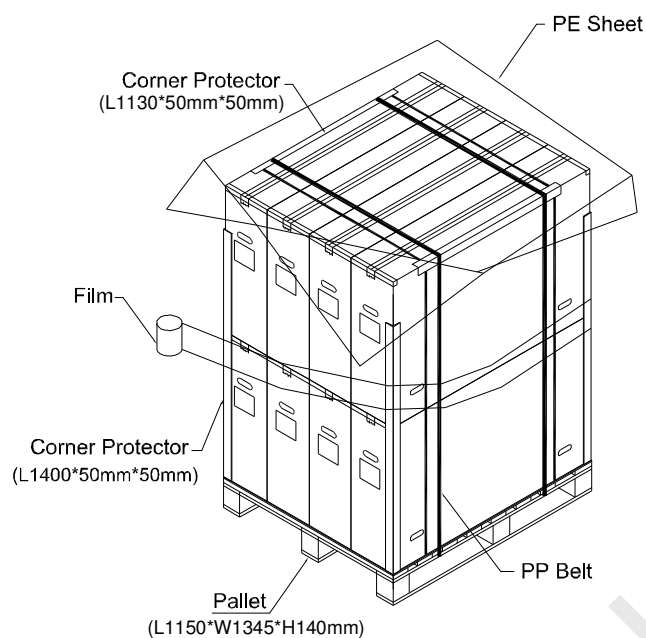


Figure.9-1 packing method

Sea & Land Transportation
Gross : 383Kg



Air Transportation
Gross : 199Kg

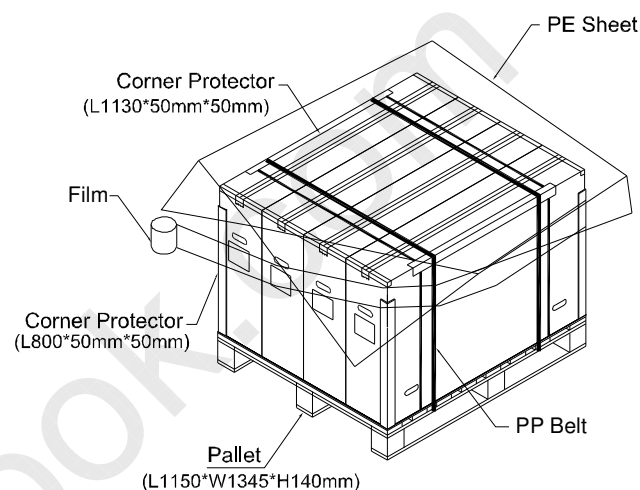


Figure. 9-2 Packing method

10. PRECAUTIONS

10.1 ASSEMBLY AND HANDLING PRECAUTIONS

- (1) Do not apply rough force such as bending or twisting to the module during assembly.
- (2) It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.
- (3) Do not apply pressure or impulse to the module to prevent the damage of LCD panel and backlight.
- (4) Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMOS LSI chips.
- (5) Do not plug in or pull out the I/F connector while the module is in operation.
- (6) Do not disassemble the module.
- (7) Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.
- (8) Moisture can easily penetrate into LCD module and may cause the damage during operation.
- (9) High temperature or humidity may deteriorate the performance of LCD module. Please store LCD modules in the specified storage conditions.
- (10) When ambient temperature is lower than 10°C, the display quality might be reduced. For example, the response time will become slow, and the starting voltage of CCFL will be higher than that of room temperature.

10.2 SAFETY PRECAUTIONS

- (1) The startup voltage of a backlight is over 1000 Volts. It may cause an electrical shock while assembling with the inverter. Do not disassemble the module or insert anything into the backlight unit.
- (2) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.
- (3) After the module's end of life, it is not harmful in case of normal operation and storage.

10.3 SAFETY STANDARDS

The LCD module should be certified with safety regulations as follows:

Regulatory	Item	Standard
Information Technology equipment	UL	UL 60950-1: 2003
	cUL	CAN/CSA C22.2 No.60950-1-03
	CB	IEC 60950-1:2001
Audio/Video Apparatus	UL	UL 60065: 2003
	cUL	CAN/CSA C22.2 No.60065-03
	CB	IEC 60065:2001

If the module displays the same pattern for a long period of time, the phenomenon of image sticking may be occurred.





CHI MEI
OPTOELECTRONICS CORP.

Issued Date: June 25, 2009

Model No.: V546H1-LE2

Tentative

